Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of fabricating a split-gate flash memory, comprising the steps of:

providing a substrate;

forming a patterned mask layer over the substrate;

forming a trench in the substrate using the patterned mask layer as an etching mask;

forming a tunnel oxide layer over the interior surface of the trench;

forming a first conductive layer inside the trench, wherein the upper surface of the first conductive layer is lower than the upper surface of the substrate;

removing the mask layer;

removing the exposed tunnel oxide layer;

forming a gate dielectric layer over the first conductive layer;

forming a conformal first dielectric layer over the substrate;

forming a second conductive layer over the substrate, wherein the second conductive layer completely fills the trench; and

forming a source/drain region in the substrate on each side of the second conductive layer.

[c2] 2. The method of claim 1, wherein the step of forming the gate dielectric layer over the first conductive layer further includes the sub-steps of:
forming a conformal second dielectric layer inside the trench;
forming a photoresist layer inside the trench, wherein the photoresist layer only partially fills the trench so that a portion of the second dielectric layer is exposed; and
removing the exposed second dielectric layer, which is not covered by the photoresist layer, to form the gate dielectric layer over the first conductive layer.

[c3] 3. The method of claim 2, wherein the gate dielectric layer includes an oxide/nitride/oxide composite layer.

[c4] 4. The method of claim 2, wherein the step of removing the exposed second dielectric layer includes wet etching.

[c5] 5. The method of claim 4, wherein the wet etching is conducted by using hot phosphoric acid as an etchant.

[c6] 6. The method of claim 1, wherein the first conductive layer serves as a floating gate.

[c7] 7. The method of claim 1, wherein the second conductive layer serves as a control gate.

[c8] 8. The method of claim 1, wherein the fabricating step

further includes forming a pad oxide layer between the patterned mask layer and the substrate.

[c9] 9. The method of claim 1, before the step of forming the trench in the substrate using the patterned mask layer as the etching mask, further comprising forming a shallow trench isolation structure in the substrate.